Our Ref.: 042390.P15934

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Terry L. Sterrett, et al.	Examiner: Chu, Chris C.
Application No.: **10/611,501**	Art Group: 2815
Filed: **June 30, 2003**	
For: **MODULAR DEVICE ASSEMBLIES**	

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Terry L. Sterrett, hereby declare that:

1. I am a citizen of the United States.
2. I currently reside at 42235 N. Tonto Drive, Cave Creek, Arizona 85331.
3. I was an employee at Intel Corporation ("Intel") in Chandler, Arizona.
4. I was employed by Intel from 1999 to 2004.
5. My title at the time I left Intel was Senior Packaging Engineer.
6. I am a co-inventor of the above-identified patent application.
7. Intel is the assignee of the above-identified patent application.
8. I have reviewed U.S. Patent No. 6,815,254 issued to Mistry, et al. ("Mistry") which was filed on March 10, 2003. The Patent Office has cited Mistry against the claims of the above-identified application.
9. The invention disclosed and claimed in the above-identified patent application was conceived in the United States of America at least as early as October 2002, as evidenced by the document Intel Invention Disclosure having ID #29382 (a copy of which is attached herein). This document was reduced to writing internally within Intel at least as early as the date on the

document, i.e., October 2, 2002. This document demonstrates conception of the claimed invention of the instant application and was prepared under my direction based on my own original work. Between October 2002 and its constructive reduction to practice by the filing of the above-captioned patent application on June 30, 2003, I directed simulations and various testing in a diligent effort to reduce the invention to practice. Therefore, the conception and diligence towards reduction to practice of the invention disclosed and claimed in the above-identified patent application occurred prior to the filing date of Mistry.

10. The document provided herewith is designated "Intel Confidential." It is Intel's practice to maintain in secrecy all documents designated "Intel Confidential." I believe that the document has at all times prior to the filing date of the above-captioned application been maintained in a confidential manner.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon.

Respectfully submitted,

Dated: June 10, 2005

Terry L. Sterrett

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INTEL CONFIDENTIAL
Attorney-Client Privileged Communication

29382

TMG INVENTION DISCLOSURE
Located at: [redacted]

TMG-TM/TMG/ATD

LEGAL ID# _____(legal dept. use only) DATE: __10-02-02_____

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to [redacted] **You can submit electronically via e-mail to "invention disclosure submission" if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call [redacted]

Fill out the below and follow the instructions:

1. **Field of the Invention:**
   - ☐ Semiconductor Process: device and integration
   - ☐ Semiconductor Process + Equipment: thin films
   - ☐ Semiconductor Process + Equipment: etch/litho
   - ☐ Circuit Design
   - ☐ Flash
   - ☐ Test
   - ☐ CQN (Q&R)
   - X Packaging
   - ☐ Boards/Cartridge
   - ☐ Automation
   - ☐ Other

2. **Concise Title of Invention:**

   Modular semiconductor device assemblies having improved interconnection designs

3. **Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention):**

   The present invention discloses the unique combination of commercially available stencil printed encapsulation processes with conventional BGA sphere interconnection technology so as to enable improved interconnection designs and encapsulation methods for modular assemblies used for multi-chip-module (MCM) devices. Specifically, the invention eliminates complicated & high-cost interconnection methods and replaces them with conventional BGA spheres and assembly techniques. The invention further discloses the usage of stencil printed encapsulation processes as a means of encapsulating multiple assembles per unit operation. The invention yet further discloses a means of improving interconnection fatigue & impact loading strength by providing a stress distributing film around interconnection spheres

   Key elements are: (1) improved & lower cost MCM interconnection designs, (2) multiple assembly encapping methods, (3) improved interconnection fatigue & impact strength, and (4) unique combination of commercially available encapsulation technologies & established interconnection methodologies enabling tailorable modular MCM assembly techniques.

4. Inventor(s):

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Division Name: ATD_X
PTD___ CTM___ CR___
STTD___ CQN ___
SMTD____TCAD___
Other?_____

Contractor:
YES _____
NO __X___

Inventor Signature:

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PTD___ CTM___ CR___
STTD___ CQN ___
SMTD____TCAD___
Other?_____

Contractor:
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NO _____

Inventor Signature:

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Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN ___
SMTD____TCAD___
Other?_____

Contractor:
YES _____
NO _____

Inventor Signature:

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)

DATE: 12/13/02 SUPERVISOR NAME: vijay wakharkar (see last page)____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?
If yes, explain and give date: [redacted]
(Give expected tape out date if applicable):

7. Has the subject matter of present disclosure been published or will it be published outside of Intel? No.
If yes, explain and give date:

8. Has a product using or manufactured using the present disclosure been sold or offered for sale?
If yes, explain and give date: No.

9. Has this invention been conceived, or constructed during accomplishment of a government or third party contract? No. If yes, give contract name and number:

10. Explain the problem being addressed by the invention:

This invention addresses the problem of forming low cost – high reliability interconnections between multichip modules. The invention eliminates the usage of high cost and complicated interposer structures to achieve inter-module connection. The invention also discloses a method of encapsulating multiple modules and forming stress-distributing films around interconnections so as to improve fatigue life and impact strength.

11. Explain current state of the art (i.e, how the problem is solved today):

Presently the problem described above is solved by first forming an interposer module from laminate material in which Cu pillars are implanted and then Sn plated. Manufacture of the interposer requires multiple assembly steps requiring high precision. The success of prior art methods depend on multiple lamination processes in which the interposer structure is laminated to substrate surfaces. In practice this has proven to be costly and a source of structural failure at the interposer – substrate interface due to poor adhesion.

12. Explain technical advantages of the invention over current state of the art:

The technical advantage of this invention is that it uses conventional BGA solder sphere technology to form intermodule interconnection. The invention further provides the technical advantage of providing a means to improve interconnection fatigue life & impact strength by providing a stress distributing film surrounding interconnection spheres. The invention yet further provides the technical advantage of providing a means of dispensing encap to multiple wirebond assemblies per unit operation as well as patterning encap dispense so as to provide a means of placing encap in specific areas in order to have a wider breadth of interconnection options. In its entirety the present invention provides a means of inexpensively producing a wide range of modular subassemblies for the manufacture of stacked MCMs. While this disclosure provides examples using wirebonded die, the materials and processes can be employed for MCMs using flip chip die and/or combinations of wirebond and flip chip die.

13. a. Is the invention experimentally verified?

- BGA ball interconnect between modules and interposer has been verified. Rev-300 Next Generation Multichip Module (NGMCM) pathfinding activities for 8x5 have demonstrated intermodule connection yields on the order of ~ 77% ... indicating feasibility.
- Multiple die stencil print encapping is commercially available from DEK & KnS. The invention's incorporation of this commercially available technology seeks to decrease the overall cost of modular assembly by using conventional MMAP processes and equipment. Stencil encapping for MMAP arrays has been commercially demonstrated.
- Pilot data has been collected showing improved BGA sphere stress distribution via film partially encapsulating spheres. Invention provides a means of partially encapping interconnection BGA spheres through stencil & encapping design. Pilot data has been collected showing that encapsulating BGA spheres increases shear strength.

b. Is the invention verified with simulation?

- Models showing improved stress distribution disclosed by present invention are scheduled to start [redacted].
- Initiated [redacted] for prototyping / demonstrating MMAP encap dispense for NGMCM packages. ECD ww46.

c. If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):

14. Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):

The present invention provides an improved method and device for forming MCM interconnections. The invention further discloses a means by which modular components comprising MCM assemblies can be simply and inexpensively produced in mass using conventional MMAP packaging processes and materials. See Figures 1 – 9 further detail.

Referenced sketches/dwg's/diagrams: (use additional page(s))

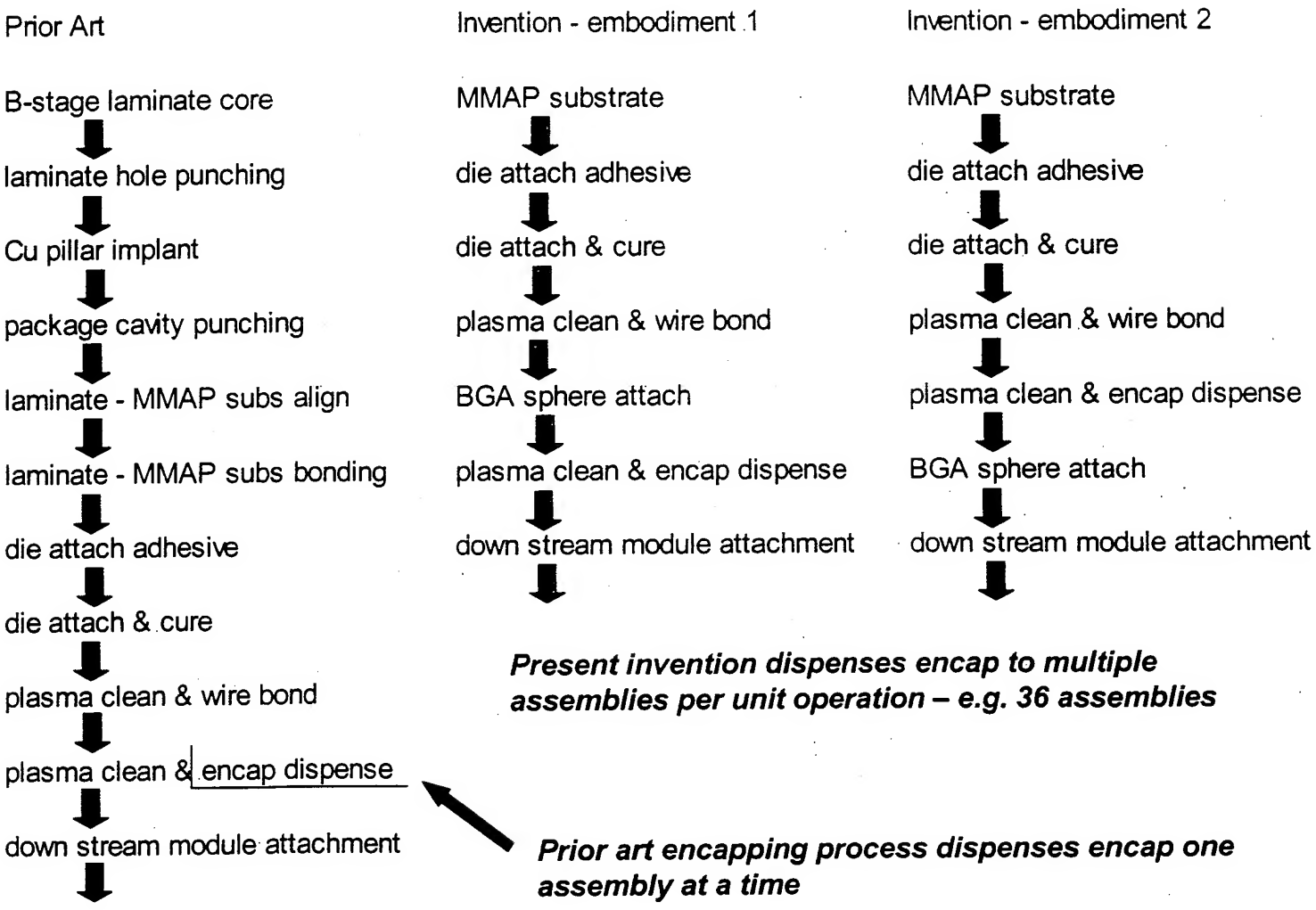
15. Prior Art (often this is helpful to explain your invention, but it is not required).

See Figures 1 – 9 for details.

The Invention (use additional figures as needed to show details and additional embodiments)

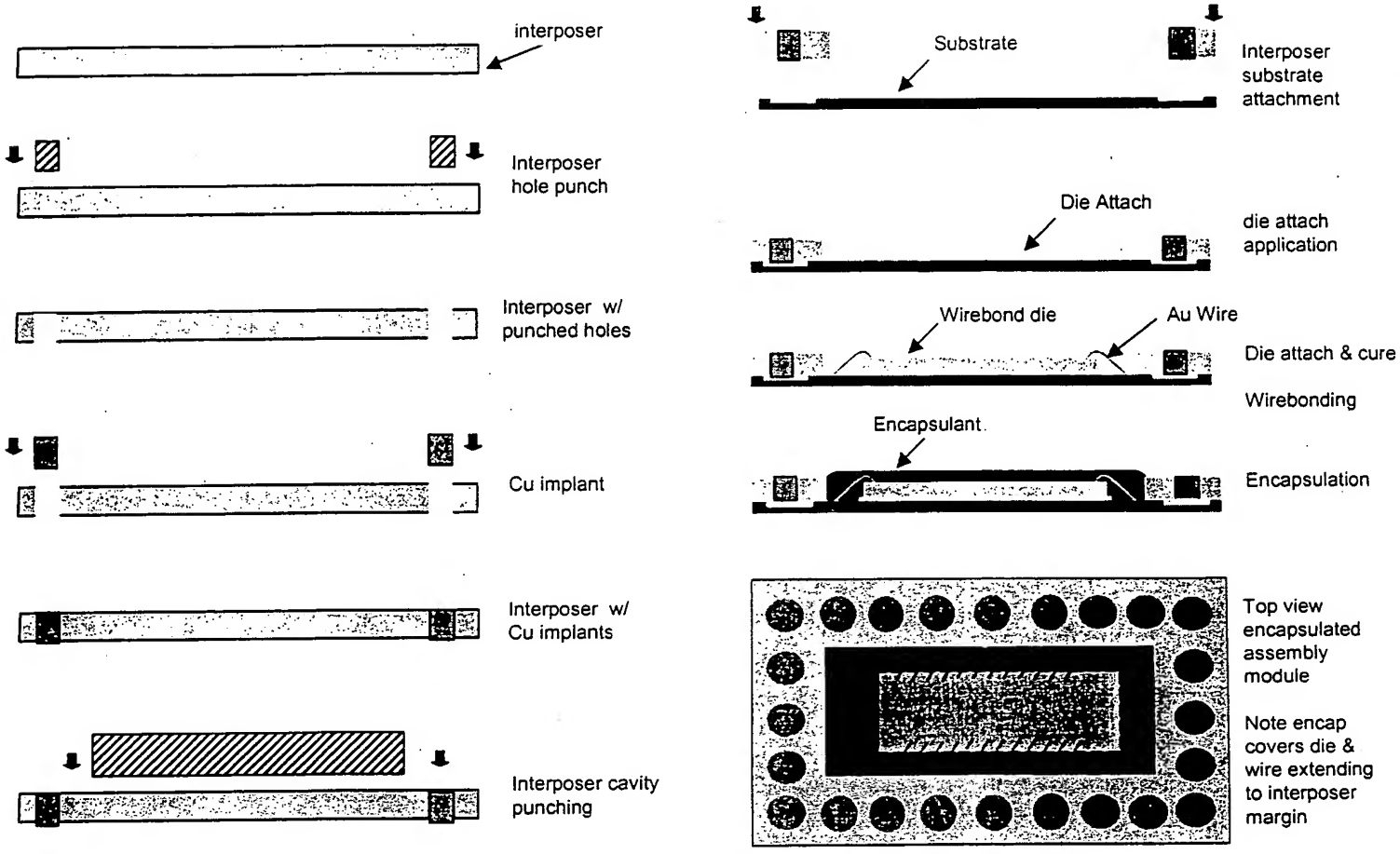
See Figures 1 – 9 for details.

Figure 1. Process flow comparison.



Present invention eliminates usage of laminate interposer as means of forming intermodule interconnection. Prior art process relies on complicated and costly process steps whereby an interposer structure having copper implants is first formed and then laminated to a module substrate surface. This process has a relatively high cost and requires strict process control in order to form optimal adhesion between interposer and substrate. Prior art devices further rely on the presence of the interposer to act as a dam for module die encapsulation. In practice, this has proven to be difficult to control leading to excessive encap bleed onto the interposer surface leading to interference with module attachment. The present invention replaces prior art laminate interposer with conventional BGA solder spheres and processes. Applicants have found that usage of commercially available stencil printed encapping processes further provide a means of encapsulating module die assemblies such that BGA spheres can be attached either prior to encapping or after encapping depending on product requirements. This flexibility allows for a wider scope of process applicability across multiple product platforms and devices.

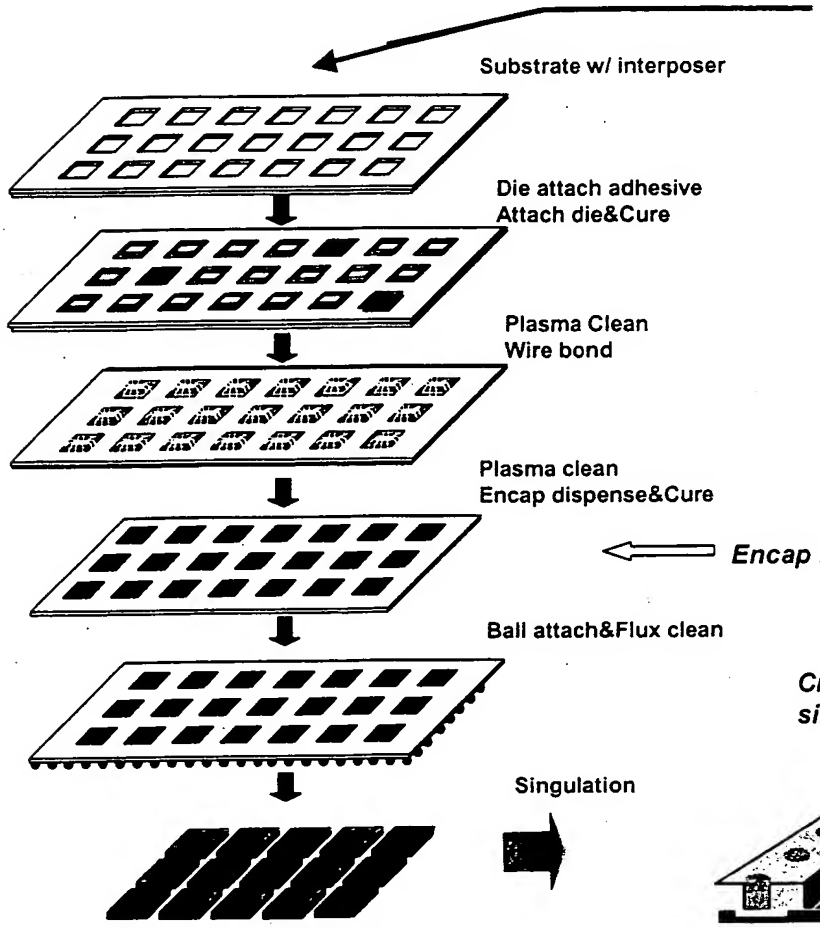
Figure 2. Prior Art Process flow and resultant module.



Prior art MCM with interposer connection

Prior art assembly process starts with interposer fabrication comprising the steps of (1) laminate formation, (2) implant punching, (3) Cu pillar implanting, (4) interposer cavity punching, (5) interposer-substrate lamination, (6) die attach adhesive dispense, (7) chip attach, (8) wirebond, (9) encapsulation, (10) singulation. A substantial amount of activity is spent preparing and attaching the interposer structure used for interconnection (e.g. steps 1-5). Lamination of the interposer to substrate is accomplished at relatively high temperatures (~200C) and pressures. The bond joint between laminate and substrate has been found to be prone to delamination.

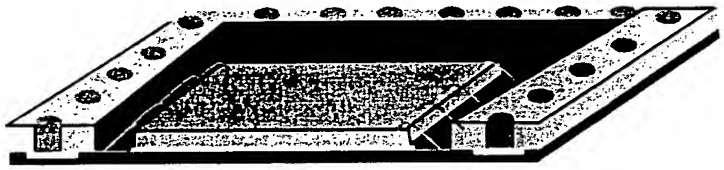
Figure 3. Prior Art Multiple Assembly Process flow and resultant module.



Note: Diagram does not show the 5 interposer assembly steps comprising implant & cavity punching, Cu pillar implanting, & interposer laminating. The diagram starts with interposer laminated to substrate

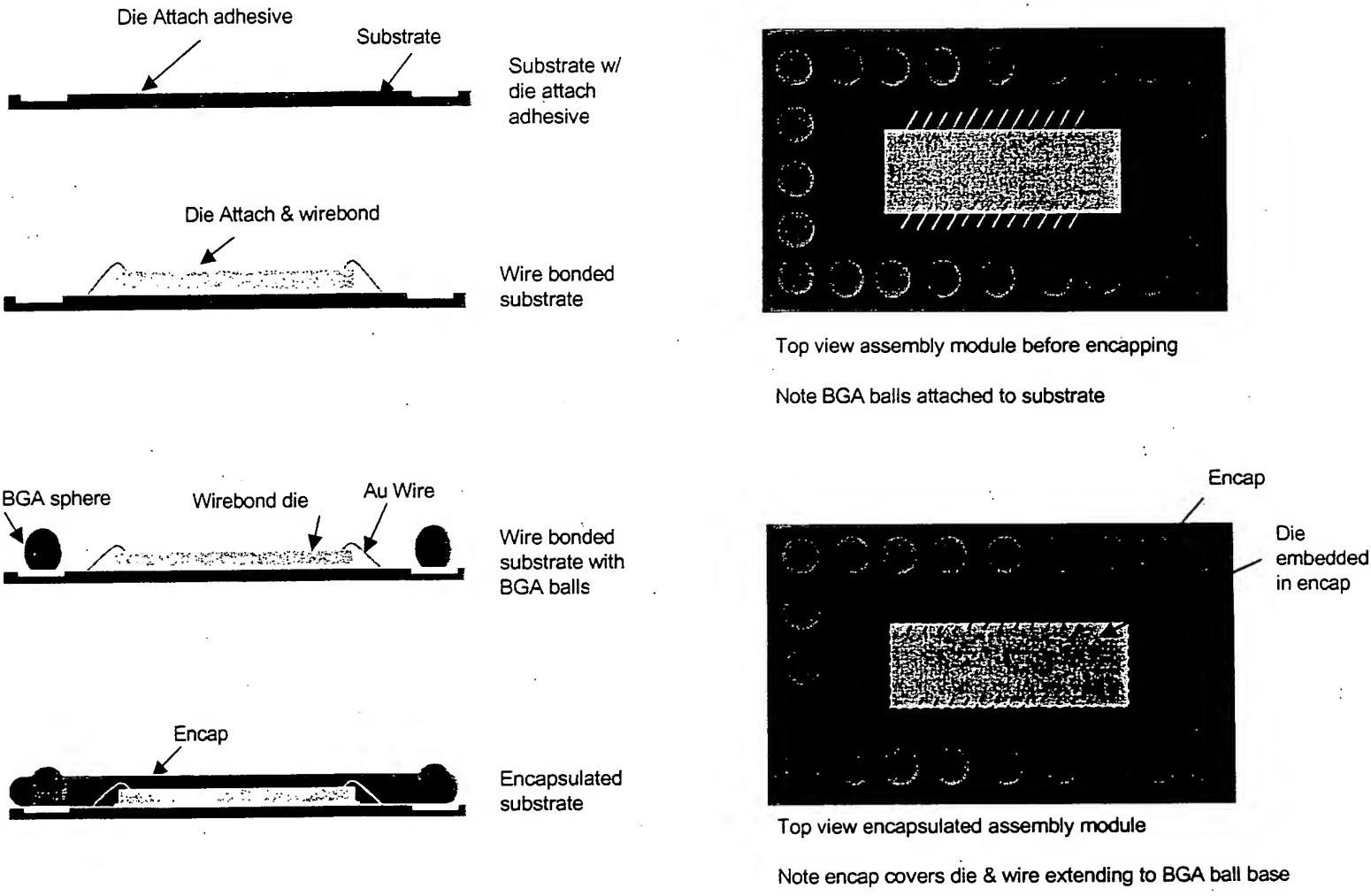
Encap is dispensed one assembly at a time

Cross section perspective view of prior art assembly after singulation



Subsequent to interposer assembly steps the prior art assembly process employs conventional wirebonding processes where encapsulation is performed on a unit per unit basis. Process throughput is relatively low and the ability to control encapsulation height is difficult. Prior art design rules require larger x-y dimensions between die and interposer in order to have sufficient room to perform wirebonding.

Figure 4. Present Invention Process flow and resultant module – embodiment 1



Embodiment 1 of the present invention – partially encapsulated interconnection spheres.

In this particular embodiment of the invention the encapsulant is used for dual purposes of providing partially encapsulated BGA spheres in order to form a stress distributing film as well as encapsulating die. This particular aspect of the invention is enabled by using commercially available stencil printing encapsulation technology such as that available from DEK and Kulicke & Soffa (KnS) under the trade name StenSEAL™, where encapsulant is pattern printed onto individual MCM subassemblies. Referring to Figure 4 there is shown a process and resultant modular device where BGA spheres are attached to upper substrate surface of conventional wirebond assemblies where encapsulant is stencil printed onto the substrate surface thereby encapsulating the wirebond die as well as partially encapsulating BGA spheres. The process and resultant device eliminates the usage of prior art interposer as a means of forming interconnection and instead employs conventional BGA solder spheres and process technology to form interconnection.

The encapping process used by the invention was developed by DEK – KnS for the assembly and encapsulation of wirebonded assemblies using micro-fine wire. As such, encapsulation is oriented from the upper assembly surface downward onto the assembly so as to minimize adverse affects onto the wire such as wire-sweep. See Figure 7 for further detail.

Through the unique combination of this well established interconnection technology with the recently developed stencil printed encapsulation processes modular subassembly components can be made so as to meet a wide range of product designs and requirements with a minimal investment in tooling and equipment. The process further provides a method of using encapsulant as a means of partially embedding interconnection BGA spheres in encapsulant material in order to form a stress distributing film layer to improve interconnection reliability.

Referring to Figure 5 below, the process of forming multiple MCM subassemblies having BGA sphere interconnections is described. Using conventional molded matrix array packaging (MMAP) assembly designs, multiple MCMs are first die attached, wirebonded, and provided BGA spheres using standard MMAP processes and materials. Once, BGA spheres are attached, encapsulant is stencil printed onto multiple MCM subassemblies in accordance with design and interconnection requirements. Subsequent to encapsulation, MCMs are singulated yielding MCM modules for down stream assembly.

The assembly methods taught by the present invention do not an extensive set of dedicated hard tooling but in stead rely on existing process links (e.g. stencil printers and BGA sphere placers) and materials that can be quickly and cheaply changed to accommodate product requirements (e.g. stencil and soft tooling changes).

Figure 5. Present Invention Process flow and resultant module – embodiment 1

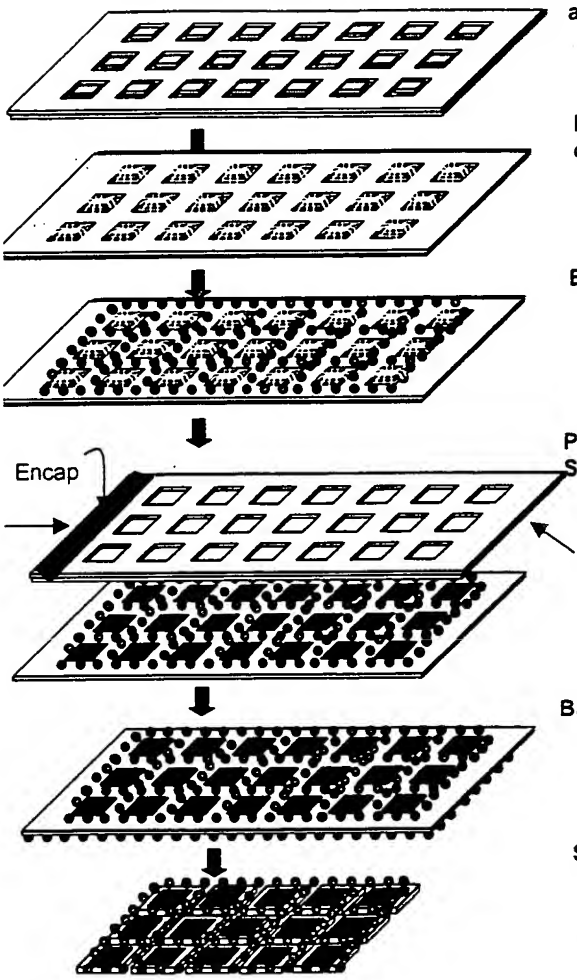


Diagram outlines process / assembly steps for embodiment 1 of the invention. The process employs stencil printing as a means of encapsulating groups of die in an array pattern.

Encap is dispensed multiple assemblies per unit operation

Cross section perspective view of present invention assembly (embodiment 1) after singulation

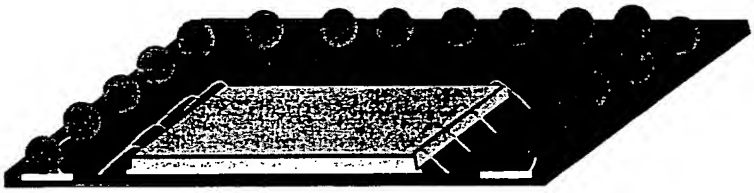
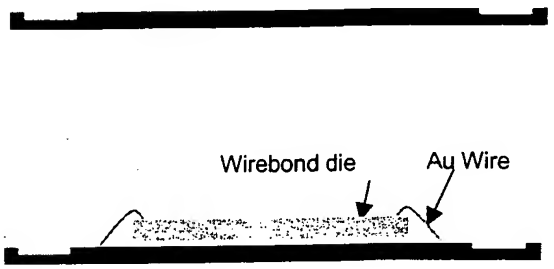
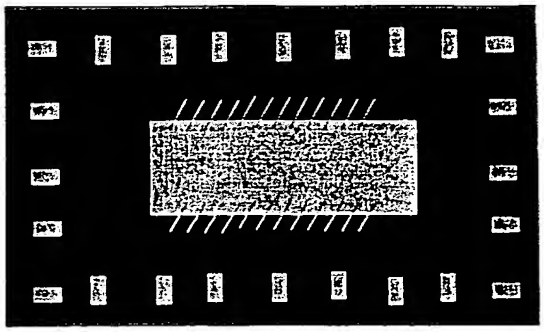


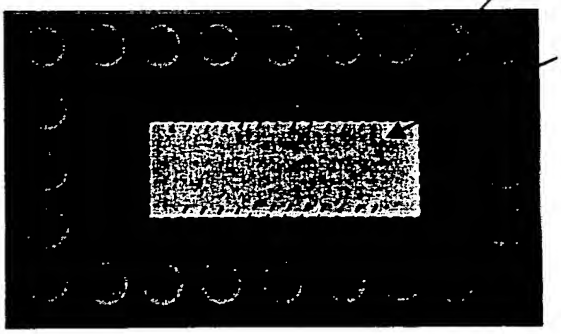
Figure 6. Present Invention Process flow and resultant module – embodiment 2





Top view assembly module before encapping

Note BGA balls not attached to substrate



Top view encapsulated assembly module

Note encap only covers die & wire

In a second embodiment of the invention, BGA interconnection spheres are attached after encapsulation. As a result, the benefits of partially encapsulating the spheres is not provided. While this benefit is absent from this particular embodiment of the invention, it does however, provide the ability to further increase throughput because tolerance. This embodiment is therefore preferred for those assemblies where BGA sphere fatigue is known to be non-critical.

Figure 7. Present Invention stencil print detail and resultant module

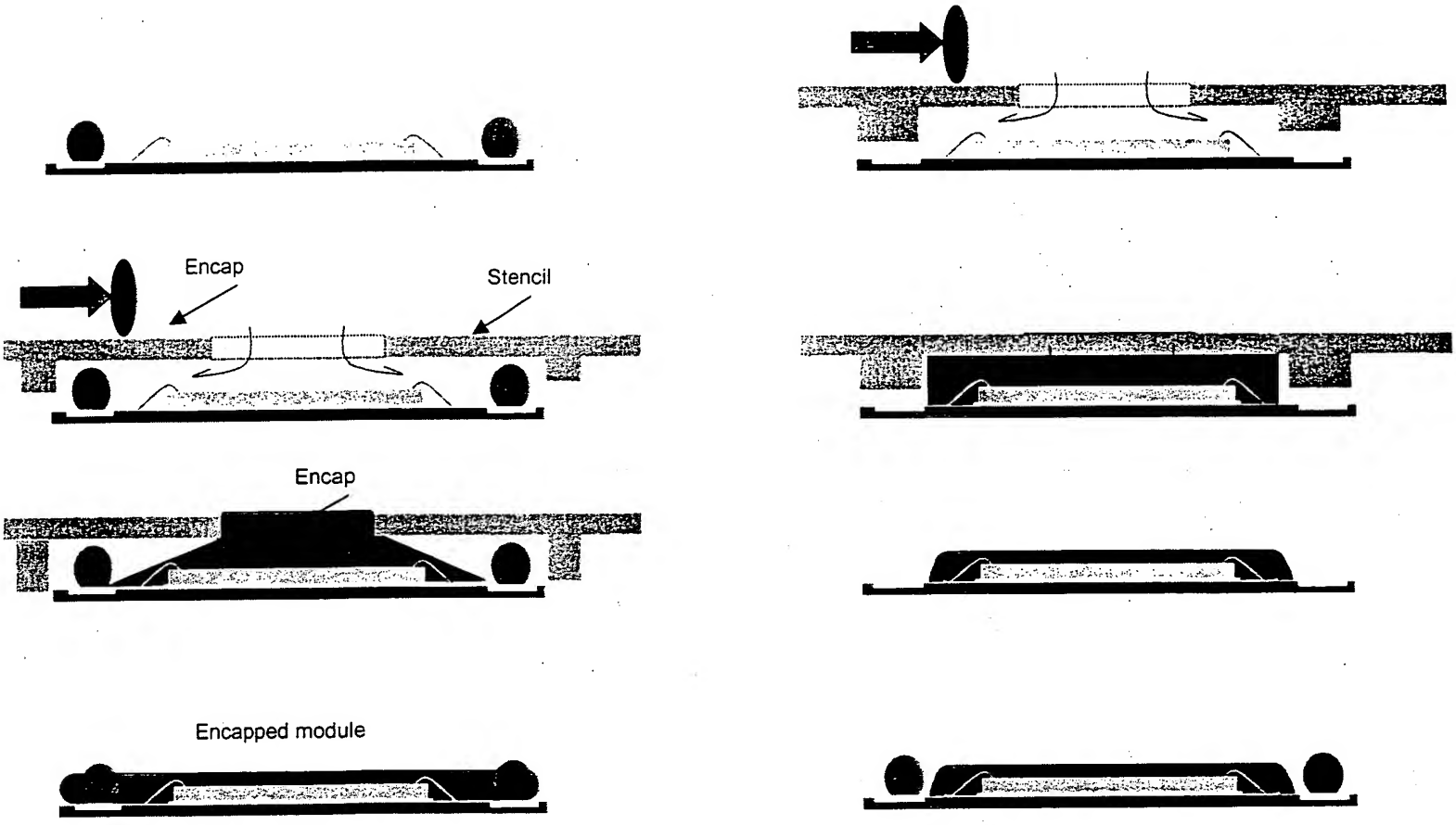
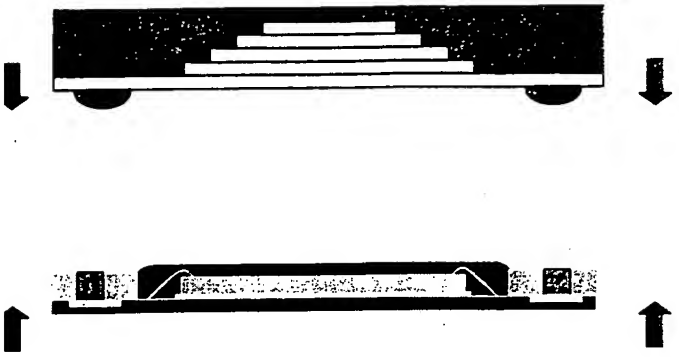


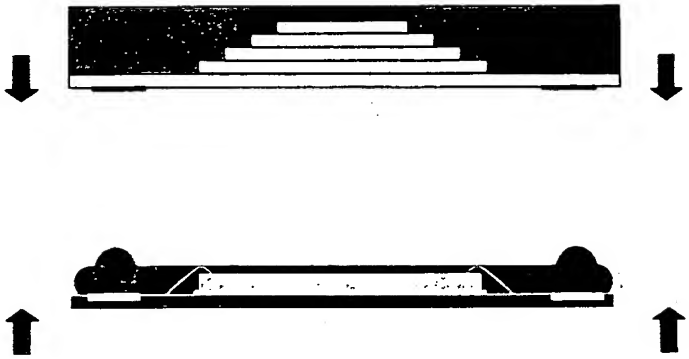
Figure 7 provides detail of stencil printed encapsulation. StenSEAL™ process developed by DEK & KnS incorporates stencil designs where the stencil acts as a dam thereby directing precise material placement. The technology, further provides a means of encapsulating micro-fine wire bonds because the material is introduced from the topside of the assembly under low pressure, low speed, laminar flow.

Figure 8. Comparison of MCM assembly .

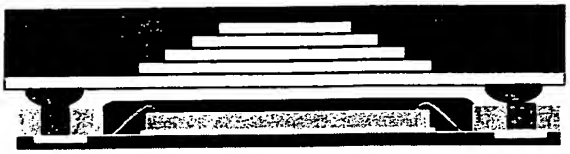
Prior art intermodule attachment



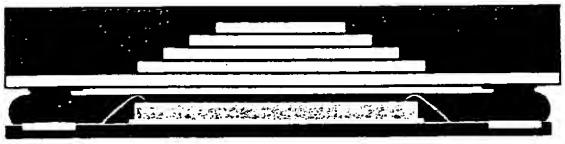
Present invention embodiment 1 intermodule attachment



Prior Art Modular Multichip Assembly



Present Invention embodiment 1 Modular Multichip Assembly



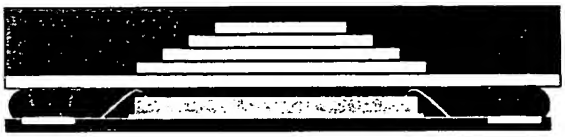
As mentioned earlier, prior art MCM assemblies employ laminate interposer structures to for m interconnection between modules. The usage of such structures has proving to be somewhat complicated, relatively expensive, and a potential source for failure. Prior art assembly method also, necessitates the application of interconnections on both upper and lower modules. For example, it is quite common that upper modules be equipped with BGA spheres corresponding to interposer connections in order to form an interconnection joint between modules. In contrast, the invention eliminates interposer structure and applies BGA sphere only to on module surface thereby eliminating duplicative processing steps. The process further improves reliability by employing well-known, conventional BGA methods and materials, where reliability is further enhance via usage of the stress distributing film disclosed by the invention.

Figure 9. Further embodiments of present invention.

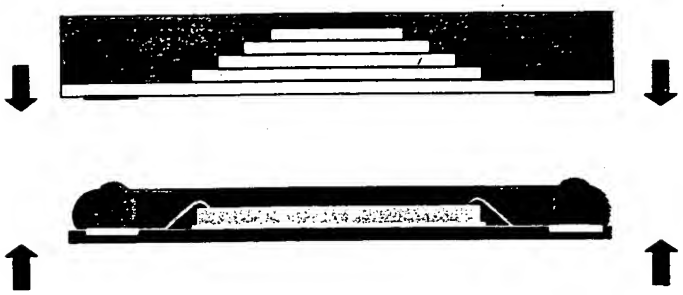
Present invention alternative embodiment 1 where encap material is B-staged so as to act as combination intermodule bonding adhesive and encap

Final encap height is within 75 to 90% of BGA ball height. Encap is B-staged to 60 to 90% of theoretical crosslink density such that material has sufficient tack to add with assembly

As BGA ball collapses during intermodule attachment, B-stage encap / bonding adhesive bonds modules together



Intermodule attachment



Present invention allows for means of coupling upper and lower modules through the use of encap material. In the example given above, encap material is B-staged and possesses resin curing chemistry such that the material begins to complete its crosslinking reaction at a time and temperature above that needed for BGA metallurgical joint formation.